1. An apparatus for characterizing an insulating layer constructed between a conductive gate and a substrate, comprising:

at least one test structure formed at a surface of a substrate, each test structure comprising:

a bulk region formed of a semiconductor within said surface,

at least one source region within the bulk region,

at least one drain region within the bulk region such that each drain region is placed at a distance from one of the source regions,

a thin insulating layer placed above the each source region, each drain region, and the bulk region between said source region and said drain region, and

the conductive gate placed above the thin insulating layer; and

a capacitance-voltage measuring device having a sense probe in contact the conductive gate of each test structure, a stimulus probe in contact with the source and drain region of each test structure to measure a capacitance value of said test structure, and a bulk biasing probe to force said bulk region between said source and drain region to a second voltage level, whereby said second voltage level forces said bulk region to an inversion,

said capacitance-voltage measuring device varying a first voltage at said source and drain region to force said test structure into the inversion state and measuring a first capacitance of said test structure.

2. The apparatus of claim 1 further comprising an insulating layer thickness calculator in communication with the capacitance-voltage measuring device to receive the capacitance as measured and from said capacitance determine the thickness of said insulating layer.

3. The apparatus of claim 1 wherein the bulk biasing probe forces the bulk region to the second voltage level equal to said first voltage and said capacitance-voltage measuring device measures a second capacitance of said test structure, a parasitic capacitance of said test structure being a difference between the second capacitance and the first capacitance.

4. The apparatus of claim 1 wherein the test structure has an area of less than $10{,}000\mu m^2$.

5. The apparatus of claim 1 wherein the test structure has an area of less than $1{,}000\mu m^2$.

6. The apparatus of claim 1 wherein the insulating layer thickness is less than 22Å.

7. A apparatus for determining thickness of an insulating layer constructed between a conductive gate and a substrate, comprising:

at least one test structure formed at a surface of a substrate, each test structure comprising:

a bulk region formed of a semiconductor within said surface,

at least one source region within the bulk region,

at least one drain region within the bulk region such that each drain region is placed at a distance from one of the source regions,

a thin insulating layer placed above the each source region, each drain region, and the bulk region between said source region and said drain region, and

the conductive gate placed above the thin insulating layer;

a capacitance-voltage measuring device having a sense probe in contact the source region and the drain region of each test structure, a stimulus probe in contact with the source and drain region of each test structure to measure a capacitance value of said test structure, and a bulk biasing probe to force said bulk region between said source and drain region, said capacitance-voltage measuring device varying a first voltage level between

said stimulus probe and said sense probe said bulk biasing probe to a second voltage level to force said test structure into an inversion state and measuring a first capacitance of said test structure; and

an insulating layer thickness calculator in communication with the capacitance-voltage measuring device to receive the capacitance as measured and from said capacitance, determines the thickness of said insulating layer.

8. The apparatus of claim 7 wherein the bulk biasing probe forces the bulk region to the second voltage level to be equal to said first voltage and said capacitance-voltage measuring device measures a second capacitance of said test structure, a parasitic capacitance of said test structure being a difference between the second capacitance and the first capacitance.

9. The apparatus of claim 7 wherein the test structure has an area of less than $10{,}000\mu m^2$.

10. The apparatus of claim 7 wherein the test structure has an area of less than $1{,}000\mu m^2$.

11. The apparatus of claim 1 wherein the insulating layer thickness is less than 22Å.

12. A method for characterizing an insulating layer constructed between a conductive gate and a substrate, comprising the steps of:

forming at least one test structure at a surface of a substrate by the steps of:

forming a bulk region of a semiconductor within said surface,

creating at least one source region within the bulk region,

creating at least one drain region within the bulk region such that each drain region is placed at a distance from one of the source regions,

constructing a thin insulating layer above the each source region, each drain region, and the bulk region between said source region and said drain region, and

placing the conductive gate above the thin insulating layer; and

performing a capacitance-voltage measurement by the steps of:

connecting the source region with the drain region of each test structure,

placing a sense probe in contact the conductive gate of each test structure,

placing a stimulus probe in contact with the source and drain region of each test structure to measure a capacitance value of said test structure,

varying a first voltage between said stimulus probe and said sense probe to force said test structure into an inversion state,

placing a bulk biasing probe in contact with said bulk region to force said bulk region between said source and drain region to a second voltage to insure said inversion state,, and

measuring a first capacitance of said test structure.

13. The method of claim 13 further comprising the step of:

determining the thickness of said insulating layer from said first capacitance.

14. The method of claim 13 further comprising the steps of:

forcing the bulk region the second voltage level equal to said first voltage, and

measuring a second capacitance of said test structure,

calculating a parasitic capacitance of said test structure as a difference between the second capacitance and the first capacitance.

15. The method of claim 13 wherein the test structure has an area of less than $10{,}000\mu m^2$.

16. The method of claim 13 wherein the test structure has an area of less than $1{,}000\mu m^2$.

17. The method of claim 13 wherein the insulating layer thickness is less than 22Å.

18. A method for determining thickness of an insulating layer constructed between a conductive gate and a substrate, comprising the steps of:

forming at least one test structure at a surface of a substrate by the steps of:

forming a bulk region of a semiconductor within said surface,

creating at least one source region within the bulk region,

creating at least one drain region within the bulk region such that each drain region is placed at a distance from one of the source regions,

constructing a thin insulating layer above the each source region, each drain region, and the bulk region between said source region and said drain region, and

placing the conductive gate above the thin insulating layer; and

performing a capacitance-voltage measurement by the steps of:

connecting the source region with the drain region of each test structure,

placing a sense probe in contact the conductive gate of each test structure,

placing a stimulus probe in contact with the source and drain region of each test structure to measure a capacitance value of said test structure, and

placing a bulk biasing probe in contact with said bulk region between said source and drain region,

varying a first voltage at said source and drain region to force said test structure into an inversion state,

forcing said bulk region to a second voltage to insure said inversion state, and

measuring a first capacitance of said test structure; and

determining the thickness of said insulating layer from said first capacitance.

19. The method of claim 18 further comprising the steps of:

forcing the bulk region to a second voltage level equal to said first voltage, and

measuring a second capacitance of said test structure,

calculating a parasitic capacitance of said test structure as a difference between the second capacitance and the first capacitance.

20. The method of claim 18 wherein the test structure has an area of less than 10,000μm^2.

21. The method of claim 18 wherein the test structure has an area of less than 1,000μm^2.

22. The method of claim 18 wherein the insulating layer thickness is less than 22Å.

23. A method for measuring capacitance-voltage curves for a transistor, comprising the steps of:

providing a substrate having a well area having at least one isolation region and a well pick-up contact therein and the transistor thereon,

said transistor comprising a gate, a gate dielectric, and source/drain regions;

measuring a first capacitance-voltage curve of the transistor under inversion and accumulation conditions by the step of:

applying a direct current signal and an alternating current signal between the gate and a common connection of the source/drain regions and the well pick-up contact; and

measuring a second capacitance-voltage curve of the transistor under inversion conditions by the steps of:

applying the direct current signal and the alternating current signal between the gate and the source/drain regions, and

floating the well pick-up contact.

24. The method of claim 23, further comprising the step of:

determining a parasitic capacitance by the step of:

obtaining a capacitance difference between the first and second capacitance-voltage curves under inversion condition.

25. The method of claim 24, further comprising the step of:

determining the second capacitance-voltage curve under the accumulation condition by the difference between the first capacitance-voltage curve under the accumulation condition and the capacitance difference.

26. A method of measuring capacitance-voltage curves for a transistor, comprising the steps of:

providing a substrate having a well area having at least one isolation region and a well pick-up contact therein and the transistor thereon,

said transistor comprising a gate, a gate dielectric, and source/drain regions;

measuring a first capacitance-voltage curve of the transistor under inversion and accumulation conditions by the step of:

applying a direct current signal and an alternating current signal between the gate and a common connection of the source/drain regions and the well pick-up contact; and

measuring a second capacitance-voltage curve of the transistor under inversion conditions by the steps of:

applying the direct current signal and the alternating current signal between the gate and the source/drain regions, and

applying a second direct current signal to the well pick-up.

27. The method of claim 26, further comprising the step of:

determining a parasitic capacitance by the step of:

obtaining a capacitance difference between the first and second capacitance voltage curves under inversion condition.

28. The method of claim 27, further comprising the step of:

determining the second capacitance-voltage curve under the accumulation condition by the difference between the first capacitance-voltage curve under the accumulation condition and the capacitance difference.

29. A method of measuring capacitance-voltage curves for a MOS transistor, comprising the steps of:

providing a substrate having a well area having at least one isolation region and a well pick-up contact therein and the MOS transistor thereon,

measuring a first capacitance-voltage curve of the MOS transistor under inversion and accumulation conditions by the step of:

applying a direct current signal and an alternating current signal between a gate of said MOS transistor and a common connection of source/drain regions of said MOS transistor and the well pick-up contact; and

measuring a second capacitance-voltage curve of the MOS transistor under inversion conditions by the steps of:

applying the direct current signal and the alternating current signal between the gate and the source/drain regions, and

floating the well pick-up contact.

30. The method of claim 29, further comprising the step of:

determining a parasitic capacitance by the step of:

obtaining a capacitance difference between the first and second capacitance-voltage curves under inversion condition.

31. The method of claim 30, further comprising the step of:

determining the second capacitance-voltage curve under the accumulation condition by the difference between the first capacitance-voltage curve under the accumulation condition and the capacitance difference.

32. An apparatus for measuring capacitance-voltage curves for a transistor, which comprises a well pick-up contact, a gate, and source/drain regions, comprising:

a measuring unit connected to said transistor

for measuring a first capacitance-voltage curve of the transistor under inversion and accumulation conditions by connecting the gate and the source/drain regions and the well pick-up contact for applying a direct current signal and an alternating current signal between the gate and the source/drain regions, and

for measuring a second capacitance-voltage curve of the transistor under inversion conditions by connecting the gate and the source/drain regions for the direct current signal and the alternating current signal are applied between two terminals and floating the well pick-up contact; and

a characteristic calculating unit coupled to the measuring unit for obtaining the first and second capacitance-voltage curves under and calculating a parasitic capacitance as a capacitance difference between the first and second capacitance-voltage curves under inversion condition and for determining the second capacitance-voltage curve under the accumulation condition by

the difference between the first capacitance-voltage curve under the accumulation condition and the parasitic capacitance.